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**Methods of Forming Capacitor Structures, and
Capacitor Structures**

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Methods of Forming Capacitor Structures, and Capacitor Structures

TECHNICAL FIELD

The invention pertains to methods of forming capacitor structures, and also pertains to capacitor structures.

BACKGROUND OF THE INVENTION

As silicon device sizes becoming increasingly smaller, and as a minimum feature size of CMOS devices approaches and goes below the 0.1 micrometer regime, very thin gate insulators can be required to keep the capacitance of a dynamic random access (DRAM) capacitor cell in a 30 femptofarad (fF) range. For instance, if insulators are formed of silicon dioxide, it can be necessary to keep the insulators to a thickness of less than 2 nanometers (20Å), and possibly even as thin as 1 nanometer (10Å). Further, even if the insulating material is kept to a suitable thickness, it can be required to form a very high aspect ratio, or very tall polysilicon capacitor structure, to achieve a desired capacitance in the range of 30 fF.

A commonly-used dielectric material is silicon dioxide (SiO₂). However, thin layers of silicon dioxide can have high leakage current density due to direct band-to-band tunneling current or Fowler-Nordheim tunneling current. Accordingly, high-k (dielectric constant) films such as TiO₂, Ta₂O₅, and Al₂O₃ have received interest as being possible

1 substitutions for silicon dioxide as dielectric materials in DRAM
2 capacitors. The higher dielectric constants of high-k materials can allow
3 the use of thicker insulators, which can have orders of magnitude less
4 tunneling current than a thin insulator while still yielding the same
5 capacitance value as the thin insulator.

6 A difficulty with the utilization of high dielectric constant
7 insulating materials is that the materials can have poor interface
8 characteristics with silicon, and a high density of interface states. Such
9 interface states can cause poor reliability of a capacitor structure, in that
10 they can charge with time under use conditions. The resulting electric
11 fields can cause breakdown of the thin dielectric insulators.

12 Among the materials which may have application as substitute
13 dielectric materials for DRAM capacitors are aluminum oxide, aluminum
14 nitride, and aluminum oxynitride. Such materials can be referred to
15 herein as AlO, AlN and AlON, respectively, with it being understood
16 that the compounds are described in terms of chemical constituents
17 rather than stoichiometry. Accordingly, even though aluminum oxide can
18 be described herein as being AlO, the material would typically be in the
19 form of Al_2O_3 , and the designation AlO used herein indicates that the
20 material comprises chemical constituents of aluminum and oxygen, rather
21 than indicating a particular stoichiometry of such constituents.

22 Several pertinent physical characteristics of AlO, AlN and AlON
23 are as follows. First, aluminum oxide is a direct band gap insulator

1 with a band gap of 7.6eV and a dielectric constant of from about 9 to
2 about 12, depending upon whether the material is amorphous or
3 crystalline. If the material is crystalline, the crystallographic orientation
4 can also affect the dielectric constant. Aluminum nitride has a band gap
5 of 6.2eV, and amorphous aluminum nitride has a dielectric constant of
6 from about 6 to about 9.6.

7 Work performed with AlN gate insulators indicates that AlN can
8 be used as a gate insulator in MIS-C-V structures on GaAs and silicon.
9 Further, it has been shown that the deposited AlN films can be oxidized
10 to form an aluminum oxide layer. Such oxidation can fill pin holes in
11 the gate insulator to avoid shorted device structures, in a similar way
12 that SiON insulators can be utilized in conventional DRAM capacitor
13 cells.

14 Aluminum nitride films can be grown epitaxially on silicon utilizing
15 metal organic chemical vapor deposition (MOCVD). Alternatively,
16 aluminum nitride films can be deposited by RF magnetron sputtering.
17 Regardless of how the aluminum nitride films are formed, they can
18 subsequently be oxidized by, for example, exposing the films to oxygen
19 at a temperature of from about 800°C to about 1,000°C for a time of
20 from about one hour to about four hours. The aluminum nitride films
21 can be oxidized either partially or fully into Al_2O_3 , depending on the
22 initial thickness of the films, the oxidation temperature, and the time of
23 exposure to the oxidation temperature.

1 The above-described methods for deposition of aluminum nitride
2 would typically be considered to be high temperature methods, and would
3 utilize temperatures of 1000°C or greater. Processes have also been
4 developed for deposition of aluminum nitride films which utilize
5 temperatures of less than 1000°C. Such processes comprise nitrogen
6 implantation into aluminum films, and can, for example, utilize ion beams
7 of nitrogen having beam energies in the range of 200 eV to 6 keV, and
8 current densities up to 50 $\mu\text{A}/\text{cm}^2$. Such densities can be produced by
9 a Penning source type ion gun with a magnetic lens. Also, aluminum
10 nitride can be formed by MOCVD, or by electron cyclotron resonance
11 (ECR) dual-ion-beam sputtering, as well as by ion-beam assisted
12 deposition (IBAD) using a nitrogen ion beam energy of 0.1 keV, 0.2
13 keV, or 1.5 keV. Still other methods for deposition of aluminum nitride
14 films include low-voltage ion plating with reactive DC-magnetron
15 sputtering, and reactive sputtering.

16 Aluminum oxynitride can also be deposited by processes utilizing
17 temperatures of less than 1000°C. For instance, aluminum oxynitride can
18 be chemical vapor deposited utilizing AlCl_3 , CO_2 and NH_3 as reactive
19 gases in a nitrogen carrier, with the films grown from the mixed gases
20 at a temperature of, for example, from 770°C to 900°C. Further,
21 aluminum oxynitride films can be grown by electron cyclotron resonance
22 plasma-assisted chemical vapor deposition.

1 Studies indicate that thin films of aluminum nitride, aluminum
2 oxynitride, and aluminum oxide can be deposited by evaporation of
3 aluminum nitride and simultaneous bombardment with one or both of
4 nitrogen and oxygen. Also, aluminum nitride and aluminum oxynitride
5 films have been prepared by ion assisted deposition, in which aluminum
6 was electron-beam evaporated on a substrate with simultaneous nitrogen
7 ion bombardment. Aluminum oxynitride films can also be formed by
8 planar magnetron sputtering from an alumina target in a mixture of
9 nitrogen and oxygen, and can be formed by reactive RF sputtering in a
10 mixture of N_2 and O_2 . Also, aluminum oxynitride diffusion barriers have
11 been formed in a temperature range of from about $400^\circ C$ to about
12 $725^\circ C$ by annealing silver/aluminum bi-layers on silicon dioxide substrates
13 in an ammonia ambient.

14 Finally, aluminum nitride can be formed by plasma nitridation of
15 metallic aluminum. The aluminum nitride can then be converted to
16 aluminum oxide, or aluminum oxynitride, by exposure of the aluminum
17 nitride to an oxygen plasma.

18 Aluminum nitride films have previously been grown on aluminum
19 films by RF sputter etching the metallic aluminum films in an ammonia-
20 rare gas plasma at temperatures near room temperature under relatively
21 modest applied plasma voltages. The technique has been used to form
22 oxide tunnel barriers on superconducting metals for Josephson devices.
23 The process essentially uses the plasma to generate reactive ions which

1 then interact with a metallic surface to form an oxide film. Electric
2 fields and ionic charges can be present which can control and accelerate
3 ion migration across a developing oxide film, with the thickness of the
4 oxide film increasing as a logarithm of reaction time. A steady, slow
5 rate of physical sputtering can be maintained by utilizing bombardment
6 with inert gas ions such that the growing oxide plateaus in thickness.
7 The particular thickness can depend on the oxide properties and the
8 plasma conditions. The plateau value can be reached by using
9 parametric values to grow a given thickness, and/or by growing the
10 thickness to a value greater than a desired thickness and then
11 subsequently restoring parameters which reduce the thickness to the
12 desired thickness. The oxide films formed by such procedures can be
13 exceptionally uniform in thickness and other properties.

14 It is possible to extend RF sputter etching techniques to formation
15 of aluminum nitride at temperatures of less than 200°C by utilizing an
16 ammonia reacting gas rather than diatomic nitrogen (N₂). The ammonia
17 can yield charged ions, while diatomic nitrogen produces neutrals whose
18 diffusion through nitride is unaided by the field across the nitride. The
19 concentration of charged ions produced in plasmas containing ammonia
20 gas can be much smaller than the concentration of charged oxygen ions
21 produced in an oxygen-containing plasma. Accordingly, it can be desired
22 to preclude oxygen from a nitridation plasma if it is desired to avoid
23 forming dielectric films comprised predominantly of oxygen anions. On

1 the other hand, if it is desired to form a film comprising aluminum
2 oxynitride, it will be desired to introduce oxygen in addition to the
3 nitrogen. One method of introducing oxygen in a low dose is to
4 introduce the oxygen in the form of N_2O .

5 6 **SUMMARY OF THE INVENTION**

7 In one aspect, the invention encompasses a method of forming a
8 capacitor structure. A first electrical node is formed, and a layer of
9 metallic aluminum is formed over the first electrical node. Subsequently,
10 an entirety of the metallic aluminum within the layer is transformed into
11 one or more of AlN, AlON, and AlO, with the transformed layer being
12 a dielectric material over the first electrical node. A second electrical
13 node is then formed over the dielectric material. The first electrical
14 node, second electrical node and dielectric material together define at
15 least a portion of the capacitor structure.

16 In another aspect, the invention encompasses a capacitor structure
17 which includes a first electrical node, a second electrical node, and a
18 dielectric material between the first and second electrical nodes. The
19 dielectric material consists essentially of aluminum, oxygen and nitrogen.

20 21 **BRIEF DESCRIPTION OF THE DRAWINGS**

22 Preferred embodiments of the invention are described below with
23 reference to the following accompanying drawings.

1 Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor
2 wafer fragment at a preliminary processing step of a method of the
3 present invention.

4 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a
5 processing step subsequent to that of Fig. 1.

6 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a
7 processing step subsequent to that of Fig. 2.

8 Fig. 4 is a view of the Fig. 1 wafer fragment shown at a
9 processing step subsequent to that of Fig. 3.

10 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a
11 processing step subsequent to that of Fig. 2, and shown in accordance
12 with a second embodiment method of the present invention.

13 Fig. 6 is a view of the Fig. 1 wafer fragment shown at a
14 processing step subsequent to that of Fig. 5 in accordance with the
15 second embodiment method of the present invention.

16 Fig. 7 is a diagrammatic, cross-sectional view of a semiconductor
17 wafer fragment at a preliminary processing step of a third embodiment
18 method of the present invention, and shown with numbering identical to
19 that utilized in describing the embodiment of Figs. 1-4.

20 Fig. 8 is a view of the Fig. 7 wafer fragment shown at a
21 processing step subsequent to that of Fig. 7 in accordance with the third
22 embodiment method of the present invention.
23

1 Fig. 9 is a view of the Fig. 7 wafer fragment shown at a
2 processing step subsequent to that of Fig. 7 in accordance with a fourth
3 embodiment method of the present invention.

4 Fig. 10 is a view of the Fig. 1 wafer fragment shown at a
5 processing step subsequent to that of Fig. 1, and shown in accordance
6 with a fifth embodiment method of the present invention..

7 Fig. 11 is a view of the Fig. 1 wafer fragment shown at a
8 processing step subsequent to that of Fig. 10 in accordance with the fifth
9 embodiment method of the present invention.

10 11 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

12 This disclosure of the invention is submitted in furtherance of the
13 constitutional purposes of the U.S. Patent Laws "to promote the progress
14 of science and useful arts" (Article 1, Section 8).

15 The invention encompasses new processes for forming capacitor
16 structures wherein low-temperature processing is utilized to form one or
17 more of aluminum nitride, aluminum oxynitride, or aluminum oxide
18 within a dielectric material between two capacitor plates. The low
19 temperature processing comprises forming a metallic layer of aluminum,
20 and subsequently converting the metallic layer to one or more of
21 aluminum nitride, aluminum oxynitride, or aluminum oxide. For purposes
22 of interpreting this disclosure and the claims that follow, "low
23

1 temperature" processing is to be understood as processing occurring at
2 less than or equal to 200°C.

3 Low temperature processing can provide numerous advantages for
4 formation of semiconductor device structures. For instance, studies
5 indicate that there is a tendency for fixed charges and fast states to
6 develop on or within a few angstroms of an aluminum nitride/silicon
7 interface, which can introduce some instabilities in the MIS electrical
8 characteristics and long-term stabilities. At least some of the slow and
9 fast states are attributable to the use of excessively high aluminum
10 nitride deposition temperatures, characteristic of, for example, CVD
11 processes. Such temperatures can allow for intermixing of components
12 at the interface, doping of the silicon with aluminum, and even some
13 formation of aluminum silicides. Forming aluminum nitride temperatures
14 under 300°C may serve to mitigate this problem, in that the diffusion
15 co-efficient of aluminum in silicon is roughly 10^{-24} cm²sec⁻¹. Accordingly,
16 aluminum penetration into silicon at temperatures of about 300°C or
17 below for exposure times of about 10,000 seconds will amount to only
18 a small fraction of an angstrom diffusion distance. Further, penetration
19 can be orders of magnitude less at temperatures of around 100°C to
20 about 200°C. Accordingly, it can be possible to avoid autodoping; and
21 maintain a clean, sharp interface if aluminum nitride, aluminum
22 oxynitride and/or aluminum oxide can be formed at temperatures of less
23

1 than or equal to 200°C. Further, if plasmas can be avoided, it can be
2 possible to avoid driving ions from a plasma into a silicon substrate.

3 An exemplary method of the present invention is described with
4 reference to Figs. 1-4. Referring initially to Fig. 1, a semiconductor
5 wafer fragment 10 is illustrated at a preliminary processing step of a
6 method of the present invention. Semiconductor wafer fragment 10
7 comprises a substrate 12 which can comprise, for example,
8 monocrystalline silicon lightly-doped with a background p-type dopant.
9 To aid in interpretation of the claims that follow, the terms
10 "semiconductive substrate" and "semiconductor substrate" are defined to
11 mean any construction comprising semiconductive material, including, but
12 not limited to, bulk semiconductive materials such as a semiconductive
13 wafer (either alone or in assemblies comprising other materials thereon),
14 and semiconductive material layers (either alone or in assemblies
15 comprising other materials). The term "substrate" refers to any
16 supporting structure, including, but not limited to, the semiconductive
17 substrates described above.

18 A transistor gate 14 is shown formed over substrate 12. Gate 14
19 comprises a pad oxide layer 16, a conductively doped silicon layer 18,
20 a silicide layer 20, and an insulative material 22. Pad oxide 16 can
21 comprise, for example, silicon dioxide; silicon layer 18 can comprise, for
22 example, polycrystalline silicon conductively doped with either an n-type
23 or p-type dopant; silicide 20 can comprise, for example, tungsten silicide

1 or titanium silicide; and insulative material 22 can comprise, for example,
2 silicon nitride or silicon dioxide.

3 Sidewall spacers 24 are shown formed along sidewalls of gate 14,
4 and can comprise, for example, silicon dioxide or silicon nitride.
5 Conductively-doped regions 26 and 28 are shown provided within
6 substrate 12 and adjacent transistor gate 14. Conductively-doped
7 regions 26 can be lightly doped and can correspond to, for example,
8 lightly doped diffusion regions; while regions 28 can be more heavily
9 doped, and can correspond to heavily doped source/drain regions.
10 Regions 26 and 28 can be conductively doped with either n-type or p-
11 type dopant. Gate 14 and doped regions 26 and 28 together define a
12 transistor structure 30.

13 An isolation region 29 is adjacent one of the source/drain
14 regions 28. Isolation region 29 can comprise, for example, silicon
15 dioxide, and can correspond to a shallow trench isolation region.

16 An insulative material 32 is shown formed over substrate 12 and
17 transistor structure 30. Insulative material 32 can comprise, for example,
18 borophosphosilicate glass (BPSG). Further, insulative structure 32 can
19 comprise multiple insulative materials, such as, for example, an underlying
20 layer of chemical vapor deposited silicon dioxide and an upper layer of
21 BPSG, even though layer 32 is illustrated in Fig. 1 as being a single
22 material layer.
23

1 An opening has been formed through insulative material layer 32
2 to one of the source/drain regions 28, and subsequently filled with a
3 conductive material 34. Conductive material 34 can comprise, for
4 example, a metal and/or a conductively doped silicon. In particular
5 embodiments, conductive material 34 comprises conductively-doped
6 polycrystalline silicon. The polycrystalline silicon can be conductively-
7 doped with either n-type or p-type dopant. Conductively material 34
8 ultimately comprises a first electrical node of a capacitor structure.
9 Although conductive material 34 is shown with a planar upper surface,
10 it is to be understood that conductive material 34 can have a roughened
11 surface, such as, for example, a surface of hemispherical grain polysilicon.
12 Also, although conductive material 34 is shown as a plug, it is to be
13 understood that conductive material 34 can have other shapes, such as,
14 for example, a container shape.

15 A metallic aluminum layer 36 is shown formed over conductive
16 material 34. Metallic aluminum layer 36 can be formed by, for example,
17 ion-assisted deposition of aluminum. Layer 36 preferably has a thickness
18 of from greater than 0Å to about 40Å and can, for example, comprise
19 a thickness of from about 5Å to about 15Å. The thickness of aluminum
20 layer 36 can be controlled to within about 1Å. Residual surface oxides
21 (not shown) can be removed from over an upper surface of conductive
22 material 34 prior to formation of metallic aluminum material 36 utilizing,
23 for example, a low-voltage sputter etching treatment.

1 Layer 36 is shown patterned to be provided only over conductive
2 material 34, and not over insulative material 32. Such patterning can
3 be accomplished by, for example, selective deposition of material 36 only
4 over conductive material 34, or by patterning layer 36 after non-selective
5 deposition. The patterning of non-selectively deposited material 36 can
6 be accomplished by, for example, forming a patterned photoresist block
7 (not shown) over a portion of material 36 that is on conductive material
8 34, while leaving other portions of material 36 not covered by the
9 photoresist block, and subsequently etching the uncovered portions of
10 material 36. The photoresist block can then be removed to leave the
11 structure shown in Fig. 1.

12 Referring next to Fig. 2, wafer fragment 10 is shown after metallic
13 aluminum layer 36 (Fig. 1) is exposed to conditions which convert the
14 metallic aluminum to a dielectric material 40. Such conditions can
15 convert layer 36 to one or more aluminum oxide, aluminum oxynitride,
16 or aluminum nitride. Preferably, the conditions will comprise low-
17 temperature transformation of material 36, with low-temperature being
18 defined as a temperature less than or equal to 200°C. Utilization of
19 low-temperature transformation can avoid exposure of the doped regions
20 26 and 28, or other doped regions associated with substrate 10, to
21 excessive temperatures which could cause undesired diffusion of dopant
22 from the doped regions to adjacent regions.
23

1 A thickness of dielectric material 40 can be determined from a
2 starting thickness of metallic aluminum layer 36 (Fig. 1) as well as by
3 the type of dielectric material ultimately formed. For instance, if the
4 dielectric material is aluminum nitride, then a starting thickness of
5 metallic aluminum layer 36 of about 20Å will yield a thickness of
6 dielectric material 40 of from about 28.5Å to about 31.5Å, assuming that
7 the metallic aluminum is entirely reacted. The metallic aluminum of
8 layer 36 can be converted to dielectric material 40 by one or more of
9 the methods described in the "Background" section of this disclosure,
10 including, for example, exposing layer 36 to reactive RF sputtering in an
11 ammonia/N₂O mixture; reactive RF sputtering of the aluminum in a
12 N₂/O₂ mixture; reactive RF sputtering of the aluminum in a O₂ or a CO₂
13 environment to form aluminum oxide; nitrogen implantation into the
14 metallic aluminum to form aluminum nitride; and electron cyclotron
15 resonance plasma-assisted chemical vapor deposition utilizing N₂O/N₂. An
16 exemplary process can utilize RF nitridation to form aluminum nitride
17 from the metallic aluminum. Specifically, a substrate can be maintained
18 at a temperature of about 25°C and can be exposed to plasma for a
19 time of from about 10 minutes to about 20 minutes. A feed gas to the
20 plasma can comprise at least 90% ammonia (by volume) and the
21 remainder argon. The plasma can have a dynamic plasma pressure of
22 about 10⁻² torr, and can be maintained with a potential to an RF
23 cathode plate of from about 300 volts to about 400 volts.

1 In the shown embodiment, an entirety of metallic aluminum of
2 layer 36 (Fig. 1) is converted to dielectric material 40. Such dielectric
3 material can consist essentially of, or consist of, aluminum nitride (AlN),
4 aluminum oxynitride (AlON), or aluminum oxide (AlO) (with the listed
5 compounds being described in terms of chemical constituents rather than
6 stoichiometry). The dielectric material 40 can comprise a thickness of,
7 for example, from greater than 0Å to less than 40Å, such as, for
8 example, a thickness of from 5Å to 15Å, or a thickness of from 20Å to
9 40Å, or a thickness of from 10Å to 20Å. The desired thickness can
10 depend on the dielectric constant of the dielectric material 40, and on
11 a desired capacitance of a capacitor structure ultimately formed to
12 comprise dielectric material 40. For instance, it can be desired that the
13 thickness of aluminum oxynitride or aluminum nitride be from 10Å to
14 20Å for a DRAM capacitor having capacitance in a 30fF range. The
15 relative dielectric constants of various materials are such that a layer of
16 AlN can be twice as thick as a layer of SiO₂ and have about the same
17 capacitance. Also, a layer of AlON can be twice as thick as a layer of
18 SiO₂ and have about the same capacitance. Further, a material
19 comprising a layer of AlON on a layer of AlN can be twice as thick as
20 a layer of SiO₂ and have about the same capacitance. Additionally, a
21 material comprising a layer of AlN on a layer of SiO₂ can be one and
22 one-half times as thick as a material consisting of SiO₂ and have about
23 the same capacitance.

1 Referring to Fig. 3, a conductive material 42 is formed over
2 dielectric material 40. Conductive material 42 can comprise, for example,
3 conductively doped silicon, and/or a metal. In the shown embodiment,
4 conductive material 42 is illustrated as being patterned to have sidewalls
5 coextensive with sidewalls of dielectric material 40. Such can be
6 accomplished by, for example, forming conductive material 42 to extend
7 past sidewalls of dielectric material 40, and then subsequently patterning
8 conductive material 42 with photoresist (not shown) and an appropriate
9 etch of conductive material 42. In alternative embodiments (not shown),
10 conductive material 42 can be formed to extend beyond sidewalls of
11 dielectric material 40 to define a capacitor plate which extends across
12 several capacitor structures. Conductive material 42 defines a second
13 electrical node which is spaced from first electrical node 34 by dielectric
14 material 40. Accordingly, conductive material 42 is capacitively coupled
15 with conductive material 34 through dielectric material 40; and materials
16 34, 40 and 42 together define a capacitor structure 44. Dielectric
17 material 40 can be considered to define a dielectric region operatively
18 positioned between electrical nodes 34 and 42 in the capacitor
19 construction 44 of Fig. 4.

20 Referring next to Fig. 4, a conductive interconnection 50 is formed
21 to extend through insulative material 32 and to a source/drain region 28
22 associated with transistor device 30. Interconnect 50 can comprise a bit
23 line interconnect, and accordingly can be connected to a bit line 52.

1 Accordingly, transistor 30 and capacitor 44 can comprise a DRAM
2 memory cell connected to a bit line, and forming a portion of a memory
3 array.

4 Figs. 5 and 6 illustrate an alternative embodiment of the present
5 invention. Referring initially to Fig. 5, wafer fragment 10 is illustrated
6 at a processing step subsequent to that of Fig. 2, and is shown
7 comprising a metallic aluminum layer 100 formed over dielectric
8 material 40. Metallic aluminum layer 100 can be formed utilizing
9 methodology described above for formation of metallic aluminum layer 36
10 of Fig. 1.

11 Referring to Fig. 6, aluminum layer 100 (Fig. 5) is converted to
12 a dielectric material 102. Such conversion can comprise methodology
13 similar to that described above with reference to Fig. 2 for formation of
14 dielectric material 40 from metallic aluminum layer 36. Accordingly,
15 dielectric material 102 can comprise one or more of aluminum oxide,
16 aluminum nitride, or aluminum oxynitride. In particular embodiments,
17 dielectric material 40 will comprise aluminum nitride and dielectric
18 material 102 will comprise aluminum oxide. The aluminum nitride can
19 have a thickness of, for example, from about 10Å to about 20Å, and the
20 aluminum oxide can have a thickness of, for example, from about 10Å
21 to about 20Å.

22 A conductive material 42 (which can be identical to described with
23 reference to Fig. 3) is formed over dielectric material 102 to define a

capacitor structure 104 comprising electrically conductive materials 34 and 42, as well as dielectric materials 40 and 102. A difference between the capacitor structure 104 of Fig. 6 and the capacitor structure 44 of Fig. 3 is that conductive material 42 is spaced from first dielectric material 40 by second dielectric material 102 in the construction of Fig. 6, whereas in the construction of Fig. 3 the conductive material 42 is on the dielectric material 40. A similarity between the capacitor constructions 44 of Fig. 3 and 104 of Fig. 6 is that both constructions can comprise a dielectric material 40 comprising aluminum, oxygen and nitrogen on a conductive material 34. Capacitor construction 104 can be incorporated into a DRAM cell utilizing processing similar to that described above with reference to Fig. 4. Dielectric materials 40 and 102 can be considered to together define a dielectric region operatively positioned between electrical nodes 34 and 42 in the capacitor construction 104 of Fig. 6.

Another embodiment of the invention is described with reference to Figs. 7 and 8. Referring initially to Fig. 7, wafer fragment 10 is shown at a processing step which is alternative to that of Fig. 1. Specifically, wafer fragment 10 is shown comprising a silicon dioxide layer 150 formed over conductive material 34 prior to formation of metallic aluminum layer 36. Silicon dioxide layer 150 can be formed by, for example, oxidation of an upper surface of a silicon-comprising material 34, or by chemical vapor deposition of silicon dioxide over

1 material 34. It has been found that aluminum does not react or diffuse
2 into clean, high-quality silicon dioxide at temperatures below 500°C, and
3 that even at 500°C, an aluminum-silicon reaction is not detected
4 regardless of whether there is significant amounts of water vapor, and
5 regardless of whether the exposure time is for several hours.
6 Accordingly, it is reasonable to deposit a controlled thickness of
7 aluminum over a controlled thickness of thermally grown silicon dioxide,
8 and yet to avoid interaction of the two materials.

9 It can be desired that a thickness of oxide material 150 be
10 carefully controlled, and such preferably comprises utilization of
11 methodology wherein any water utilized during formation of oxide
12 layer 150 is ultra-pure water.

13 Oxide layer 150 can be formed to a controlled thickness by
14 carefully growing the oxide layer to a desired thickness. Alternatively,
15 oxide layer 150 can be grown beyond a desired thickness, and then
16 carefully etched back to a desired thickness. One method for etching
17 back an oxide is to utilize an inductively coupled plasma optical
18 emissions spectroscopy technique, which can permit detection and
19 determination of variations in oxide thickness to within a monolayer, and
20 possibly to within 0.2Å.

21 Silicon dioxide layer 150 preferably has a thickness of from greater
22 than 0Å to less than about 15Å, and a thickness of about 10Å can be
23 preferred.

1 Referring to Fig. 8, metallic aluminum layer 36 (Fig. 7) is
2 converted to a dielectric material 152. Such conversion can comprise,
3 for example, exposing metallic aluminum layer 36 to conditions similar
4 to those discussed above with reference to Fig. 2 to form dielectric
5 material layer 152 to comprise one or more of aluminum nitride,
6 aluminum oxide, or aluminum oxynitride. In an exemplary process,
7 dielectric layer 152 can comprise aluminum oxynitride, and can be formed
8 to a thickness of from about 20 to 40Å, and silicon dioxide layer 150
9 can comprise a thickness of from about 5Å to about 15Å, with a
10 preferred thickness being about 10Å. In other exemplary processing,
11 dielectric material 152 can consist essentially of, or consist of aluminum
12 nitride, and can be formed to a thickness of, for example, from about
13 20Å to about 40Å, and silicon dioxide 150 can be formed to a thickness
14 of from about 5Å to about 15Å, with about 10Å being a preferred
15 thickness.

16 Conductive material 42, dielectric materials 150 and 152, and
17 conductive material 34 together define a capacitor construction 154.
18 Capacitor construction 154 can be incorporated into a DRAM cell
19 utilizing methodology similar to that discussed above with reference to
20 Fig. 4. Dielectric materials 150 and 152 can be considered to together
21 define a dielectric region operatively positioned between electrical nodes
22 34 and 42 in the capacitor construction 154 of Fig. 8.
23

Fig. 9 illustrates yet another embodiment of the present invention, and specifically illustrates that the methodology of Figs. 7 and 8 can be combined with that of Figs. 5 and 6. Fig. 9 illustrates wafer fragment 10 comprising a capacitor structure 162 which incorporates three dielectric material layers 150, 152 and 160. Dielectric material layers 150 and 152 can be formed by the processing described above with reference to Figs. 7 and 8. Dielectric material 160 can be formed by forming a metallic aluminum layer over dielectric material 152, and subsequently converting the metallic aluminum layer to a dielectric material. Such can be conducted analogously to the processing described with reference to Figs. 5 and 6 wherein a metallic aluminum layer 100 is formed over a dielectric material 40 and subsequently converted to a dielectric material 102. Accordingly, dielectric material 160 of Fig. 9 can comprise aluminum oxide, aluminum nitride or aluminum oxynitride, and in particular embodiments can consist of, or consist essentially of aluminum oxide, aluminum nitride or aluminum oxynitride. In particular methodology, dielectric material 150 can consist of silicon dioxide, dielectric material 152 can consist of aluminum nitride, and dielectric material 160 can consist of aluminum oxide. In such embodiment, silicon dioxide material 150 can have a thickness of from about 5Å to about 15Å, aluminum nitride material 152 can have a thickness of from about 5Å to about 15Å, and aluminum oxide material 160 can have a thickness of from about 5Å to about 15Å, with exemplary thicknesses of materials

1 150, 152 and 160 being about 10\AA each. Dielectric materials 150, 152
2 and 160 can be considered to together define a dielectric region
3 operatively positioned between electrical nodes 34 and 42 in the capacitor
4 construction 162 of Fig. 9.

5 The capacitor structure 162 of Fig. 9 can be incorporated into a
6 DRAM cell utilizing methodology similar to that discussed above with
7 reference to Fig. 4.

8 Fig. 10 illustrates yet another embodiment of the present invention,
9 and shows wafer fragment 10 at a processing step subsequent to that of
10 Fig. 1. Specifically, a metallic aluminum layer 36 of Fig. 1 has been
11 transformed to a dielectric material 170 analogously to the formation of
12 dielectric material 40 of Fig. 2. However, in contrast to the processing
13 described above with reference to Fig. 2, the formation of dielectric
14 material 170 has caused formation of a silicon dioxide layer 172 under
15 dielectric material 170. Such can occur if dielectric material 170
16 comprises aluminum oxide or aluminum oxynitride, and if oxygen utilized
17 during the transformation of metallic aluminum layer 36 (Fig. 1) to
18 dielectric material 170 permeates the aluminum layer to interact with a
19 silicon-comprising material 34 and oxidize an upper portion of the
20 material. Such can occur if, for example, an aluminum oxide or
21 aluminum oxynitride layer 170 is formed utilizing an implant of oxygen
22 into metallic aluminum layer 36. In particular processing, silicon dioxide
23 layer 172 will have a thickness of greater than 5\AA , and can, for example,

1 have a thickness of about 10Å. Also, dielectric material 170 can be
2 formed to a thickness of, for example, from about 10Å to about 40Å,
3 with an exemplary thickness being from about 10Å to about 20Å.

4 Referring to Fig. 11, subsequent processing can be utilized to form
5 a conductive material 42 over dielectric material 170, and accordingly to
6 define a capacitor construction 174 comprising conductive material 42,
7 dielectric materials 170 and 172, and conductive material 34. Capacitor
8 construction 174 can be incorporated into a DRAM cell utilizing
9 methodology similar to that discussed above with reference to Fig. 4.

10 In compliance with the statute, the invention has been described
11 in language more or less specific as to structural and methodical
12 features. It is to be understood, however, that the invention is not
13 limited to the specific features shown and described, since the means
14 herein disclosed comprise preferred forms of putting the invention into
15 effect. The invention is, therefore, claimed in any of its forms or
16 modifications within the proper scope of the appended claims
17 appropriately interpreted in accordance with the doctrine of equivalents.
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